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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,567	06/04/2001	Joseph P. Meehan	US 010229	4213

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,567	MEEHAN ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-11,13-15,17 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 13-15* is/are allowed.

6)☒ Claim(s) *4-10,17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06/04/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 05/08/2006 has been entered. Claims 4-11, 13-15, 17 and 19 are pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 05/08/2006 have been fully considered but they are not persuasive.

In response to Applicants' arguments on page 6 that "Cupo describes using only the equalizer coefficient portions of the output of the equalizers 106, 107. The data portion of the output is later merged to form output data, but is not used by the timing recovery circuit. In contrast, claim 7 recites combining the entire output (i.e., the N equalized feedback signals) of the forward equalizers 16a, 16n and feeding this output into the timing recovery circuit 20".

The Examiner's position is that Applicants arguments are not persuasive. Referring to figure 1, in column 4 lines 10-30, Cupo et al. teaches that to compensate for timing offset and drift, the frequency and/or phase of this master clock signal is altered by receiver timing generator 105 using timing adjustment signals provided by the timing recovery circuit 123. These timing adjustment signals *are a function of the delay introduced by each equalizer* to one or more predetermined nonzero frequency

components of its input signal. As suggested by Cupo et al. disclosure, because the timing adjustment signals are a function of the delay introduced by each equalizer, one of ordinary skill in the art at the time the invention was made would have recognized that the delay signal can be a combination of the equalizer outputs taking into account delay introduced by each equalizer. Coefficient updating circuits 108 109 are utilized to provide updated coefficients to equalizers 106 and 107; see column 3 lines 30-35, also FIG. 1. Contrary to Applicants' assertion that Cupo describes using only the equalizer coefficient portions of the output of the equalizers 106, 107, Cupo et al. updates equalizer coefficients and uses equalizer outputs for generating timing adjustment signals; see FIG. 1.

In response to newly added limitations "the combination of the feedback signals is used to "generate an output of the digital receiver".

The Examiner's position is that referring to FIG. 1 again, as recited above, the delay signal can be a combination of the equalizer outputs taking into account delay introduced by each equalizer. The delay signal is further use to generate timing adjustment signals provided by the timing recovery circuits 123 (see column 4 lines 15-25), wherein the clock signal for A/D converters 103 and 104 is provided by receiver timing generator 105 in response to a master clock signal furnished by master clock 122 and to timing adjustment signals provided by timing recovery circuit 123; see column 4 lines 9-20. Data output from data merge circuit 112 is generated based on the timing adjustment signals, which are function of the delay introduced by each equalizer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cupo et al. U.S. Patent 5,353,312 (previously cited).

Regarding claim 7, figure 1 discloses a receiver including:

A/D converters 103 and 104 for receiving two bit streams at first sampling rate and outputting bit streams at second sampling rate; see column 3 lines 15-35;

Adaptive equalizers 106 and 107 for generating equalized feedback signals via leads 124 and 125; see column 4 lines 10-30;

A timing recovery circuit 123 for generating a timing recovery control signal based upon the equalized feedback signals via leads 124 and 125; see column 4 lines 10-30.

Further in column 2 lines 20-35, the digital data to be transmitted is divided into two different digital signals and each signal is coupled through an associated transmission channel. At the receiver, the received version (channels A and C, see figure 1) of each transmitted signal is processed by an associated equalizer and the outputs therefrom are combined to recover the digital data. In

light of the foregoing discussion, the receiver includes two antennas for receiving the two transmitted digital signals.

Referring to figure 1, in column 4 lines 10-30, Cupo et al. teaches that to compensate for timing offset and drift, the frequency and/or phase of this master clock signal is altered by receiver timing generator 105 using timing adjustment signals provided by the timing recovery circuit 123. These timing adjustment signals *are a function of the delay introduced by each equalizer* to one or more predetermined nonzero frequency components of its input signal. As suggested by Cupo et al. disclosure, because the timing adjustment signals are a function of the delay introduced by each equalizer, one of ordinary skill in the art at the time the invention was made would have recognized that the delay signal can be a combination of the equalizer outputs taking into account delay introduced by each equalizer. Coefficient updating circuits 108 109 are utilized to provide updated coefficients to equalizers 106 and 107; see column 3 lines 30-35, also FIG. 1.

Furthermore, the delay as recited above is used to compensate for timing offset and drift for the clock signal of A/D converters 103 and 104 to generate the data output through data merge circuit 112; see column 4 lines 1-25, also FIG. 1.

Regarding claim 6, claim 6 is rejected on the same ground as for claim 7 because of similar scope. Referring to FIG. 1, dual duplex receiver 100 includes dual antennas and dual timing recovery circuits for channels A and C.

Regarding claim 17, claim 17 is rejected on the same ground as for claim 7 because of similar scope.

4. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cupo et al. U.S. Patent 5,353,312 (previously cited) as applied to claim 7 in view of figure 1 admitted prior art (previously cited) .

Regarding claim 8, Cupo et al. does not teach N carrier recovery circuits as set forth in the application claim.

On page 4 of the original disclosure, figure 1 admitted prior art discloses a receiver, as illustrated in FIG. 1, comprising a Timing Recovery (TR) circuitry employed in conventional chipsets. In FIG. 1, a digital television (DTV) receiver 1 includes a sample rate converter (SRC) 10, a carrier recovery (CR) circuit 12, a square-root raised cosine (SQRC) filter 14 (e.g., a finite impulse response (FIR) filters with a square root of a raised cosine characteristic and a forward equalizer (FE) 16.

In column 4 lines 10-30, Cupo et al. teaches that the clock signal for A/D converters 103 and 104 is provided by receiver timing generator 105 in response to a master clock signal furnished by master clock 122 and to timing adjustment signals provided by timing recovery circuit 123 as shown in figure 1. To compensate for timing offset and drift, the frequency and/or phase of this master clock signal is altered by receiver timing generator 105 using timing adjustment signals provided by the timing recovery circuit 123. In light of the foregoing

discussion, Cupo et al. teachings employ coherent detection to compensate for timing offset and drift. Because carrier offset must be estimated at the receiver if the detector is phase-coherent, therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Cupo et al. teachings can be modified to implement a carrier recovery (CR) circuit for each receiving path as taught in figure 1 admitted prior art. The implemented CR circuit for each receiving path is coupled between the A/D converter and the equalizer as disclosed in figure 1.

Regarding claim 19, claim 19 is rejected on the same ground as for claim 8 because of similar scope.

5. Claims 4-5 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langberg U.S. Patent 5,703,905 (previously cited) as applied to claim 11 above, and further in view of admitted prior art and Bernard Sklar, "Digital Communications Fundamentals and Applications" (previously cited).

Regarding claims 4-5, 9-10 and 13-14, Langberg does not teach the carrier bandpass filter being a square-root raised cosine filter as claimed in the application claim.

Figure 1 admitted prior art teaches a receiver including square-root raised cosine (SQRC) filter 14. Bernard Sklar discloses in the textbook "Digital Communications Fundamentals and Applications" on pages 100-103 that a square-root raised cosine

filtering is frequently used in digital communications because of the excellent characteristic of square-root raised cosine function for pulse shaping to reduce intersymbol interference. In light of the foregoing reason, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Langberg teachings can be modified to implement the square-root raised cosine filter. The square-root raised cosine filter is a finite impulse response filter.

Allowable Subject Matter

6. Claims 11 and 13-15 allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 11, claim is allowable after Applicant amended claim to include allowable limitations "*a timing recovery circuit generating the TR control signal based upon a selected one of the N equalized feedback signals, the combination used to generate an output of the digital receiver*".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Cong Tran 07/20/2006

Primary Examiner KHANH TRAN